CLEAN VERSION OF THE PENDING CLAIMS

1. A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;

depositing a conductive layer on said first dielectric layer, the conductive layer having an upper surface and a lower surface;

depositing an additional layer on said conductive layer;

patterning said conductive layer and said additional layer by:

forming a patterned mask layer on said additional layer; and

etching through said additional layer and said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space, the layer of dielectric material extending above the upper surface of the adjacent lines of conductive material and below the lower surface of the adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween, but not extending directly over or under the upper and lower surfaces of the adjacent lines of conductive material;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

2. The method as defined in Claim 1, further comprising the step, to be performed after said step of removing said layer of dielectric material and before said step of depositing a second dielectric layer, of removing said additional layer on said lines of conductive material.

3. The method as defined in Claim 2, wherein said additional layer comprises titanium.

4. The method as defined in Claim 2, wherein said additional layer comprises TiN.

5. The method as defined in Claim 1, wherein at least one of said first and second dielectric layers comprises silicon dioxide.

6. The method as defined in Claim 1, wherein said dielectric material comprises PTFE.

7. The method as defined in Claim 1, wherein said additional layer comprises silicon dioxide.

8. The method as defined in Claim 1, wherein said step of removing said layer of dielectric material comprises an etch back step.

9. The method as defined in Claim 1, wherein said step of removing said layer of dielectric material comprises a chemical mechanical polishing step.

10. The method as defined in Claim 1, wherein said conductive material is selected from the group consisting of polysilicon, aluminum, copper, tungsten, and multiple layers of TiN/Al/TiN, TiN/Al/Ti, W/TiN/Ti, or any combinations thereof.

11. A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;

depositing a conductive layer on said first dielectric layer, the conductive layer having a lower surface and an upper surface;

patterning said conductive layer by:

forming a mask layer on said conductive layer; and

etching through said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer that extends below the lower surface of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material each having an upper surface;

depositing an additional layer on the upper surfaces of lines of conductive material and on said first dielectric layer;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space, the layer of dielectric material extending above the upper surface of the lines of conductive material and below the lower surface of the lines of conductive material but not directly over or under the upper and lower surfaces of the lines of conductive material;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

12. The method as defined in Claim 11, wherein depositing an additional layer comprises depositing a layer of silicon dioxide by silane and oxygen based plasma enhanced chemical vapor deposition.

13. The method as defined in Claim 11, further comprising, after depositing an additional layer and before depositing a layer of dielectric material, of etching said additional layer.

14. The method as defined in Claim 13, wherein said additional layer has a top surface extending to a lateral surface at a corner, and wherein said step of performing an etch on said additional layer etches the corner of the additional layer faster than the top surface of the additional layer.

15. The method as defined in Claim 13, wherein said additional layer comprises silicon dioxide and wherein said step of performing an etch on said additional layer etches in an argon or an argon-plus-fluorine based plasma.

16. The method as defined in Claim 11, wherein at least one of said first and second dielectric layers comprises silicon dioxide.

17. The method as defined in Claim 11, wherein said dielectric material comprises PTFE.

18. The method as defined in Claim 11, wherein said additional layer comprises silicon dioxide.

19. The method as defined in Claim 11, wherein said step of removing said layer of dielectric material comprises an etch back step.

20. The method as defined in Claim 11, wherein said step of removing said layer of dielectric material comprises a chemical mechanical polishing step.

21. The method as defined in Claim 11, wherein said conductive material is selected from the group consisting of polysilicon, aluminum, and copper.

22. A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;

depositing a metal layer on said first dielectric layer, the metal layer having a lower surface and an upper surface;

patterning said metal layer by:

forming a mask layer on said metal layer; and

etching through said metal layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said metal layer that extends below the lower surface of said metal layer, said adjacent remaining portions of said metal layer forming metal lines each having an upper surface;

depositing a thin layer of silicon dioxide conformably over said metal lines and selectively on said upper surfaces of said metal lines;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space, the layer of dielectric material extending above the upper surface of the lines of conductive material and below the lower surface of the lines of conductive material but not directly over or under the upper and lower surfaces of the lines of conductive material;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

23. The method as defined in Claim 22, wherein said step of depositing a layer of silicon dioxide conformably over said metal lines and selectively on said upper surfaces of said metal lines comprises an ozone-based TEOS deposition.

24. The method as defined in Claim 22, wherein said metal lines comprise aluminum with a titanium nitride film on said upper surface of said metal lines.

25. The method as defined in Claim 22, further comprising, after depositing a layer of silicon dioxide conformably over said metal lines and before depositing a layer of dielectric material, of etching said additional layer.

26. The method as defined in Claim 25, wherein said additional layer has a top surface extending to a lateral surface at a corner, and wherein said step of performing an etch on said additional layer etches the corner of the additional layer faster than the top surface of the additional layer.

27. The method as defined in Claim 26, wherein said additional layer comprises silicon dioxide and wherein said step of performing an etch on said additional layer etches in an argon or an argon-plus-fluorine based plasma.

28. The method as defined in Claim 22, wherein at least one of said first and second dielectric layers comprises silicon dioxide.

29. The method as defined in Claim 22, wherein said dielectric material comprises PTFE.

30. The method as defined in Claim 22, wherein said additional layer comprises silicon dioxide.

31. The method as defined in Claim 22, wherein said step of removing said layer of dielectric material comprises an etch back step.

32. The method as defined in Claim 22, wherein said step of removing said layer of dielectric material comprises a chemical mechanical polishing step.

33. The method as defined in Claim 22, wherein said metal layer comprises at least one of aluminum or copper.

34. A method of forming an interlevel dielectric comprising:

providing a first dielectric layer over a surface of a substrate;

forming a conductive layer on said first dielectric layer, the conductive layer having a lower surface and an upper surface;

forming an additional layer on said conductive layer;

forming lines of conductive material having spaces therebetween that extend below the lower surface of said conductive layer from the conductive layer;

filling the spaces between the lines of conductive material with dielectric material having a dielectric constant of less than about 3.6; and

forming a second dielectric layer on the additional layer, wherein said second dielectric layer and said additional layer are formed of the same material;

wherein portions of the dielectric material having a dielectric constant of less than about 3.6 extend both above and below the adjacent lines of conductive material but do not extend directly over or under the upper and lower surfaces of the lines of conductive material.

35. A method of forming an interlevel dielectric that reduces fringe capacitance between adjacent lines of conductive material, the method comprising:

providing a first dielectric layer over a surface of a substrate;

forming a conductive layer on said first dielectric layer, the conductive layer having a lower surface;

forming an additional layer on said conductive layer;

etching through said additional layer and said conductive layer in a single etch step and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer that extends below the lower surface of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material;

filling the spaces between adjacent remaining portions of said conductive layer with dielectric material having a dielectric constant of less than about 3.6; and

forming a second dielectric layer on the additional layer, wherein said second dielectric layer and said additional layer are formed of the same material;

wherein the dielectric material having a dielectric constant of less than about 3.6 extends both above and below, but not directly over, the respective adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween.

36. (Cancelled).

~~37. The method as defined in Claim 11, wherein the layer of dielectric material having a~~ dielectric constant of less than about 3.6 extends both above and below the adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween.

38. The method as defined in Claim 22, wherein the layer of dielectric material having a dielectric constant of less than about 3.6 extends both above and below the adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween.